AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An information processing method realized in a system in which a processor including a plurality of central processing units and internal storage means, external storage means in which are stored a common code to be executed in common by the plurality of central processing units and an instruction code to be respectively executed by predetermined one of the central processing units, and host processing means are interconnected by a bus, the method characterized by comprising:

a step of loading, by means of one of the central processing units, the common code and the instruction code defined to be executed by one of the central processing units, into the internal storage means from the external storage means in accordance with an instruction from the host processing means, and loading, by means of one of other central processing units, the instruction code defined to be executed by the one of other central processing units, into the internal storage means from the external storage means; and

a step of executing the common code and the instruction code defined to be executed by the respective central processing units, which are loaded in the internal storage means, by means of the respective central processing units,

wherein the common code, the instruction code loaded by the one of the central processing units, and the instruction code loaded by the one of the other central processing units share a common address space in the internal storage means.

2. (Original) The information processing method according to claim 1, further comprising:

a step of selectively resetting the central processing units by means of the host processing means;

a step of newly loading an instruction code defined to be executed by a selectively reset one of the central processing unit, from the external storage means into the internal storage means by means of the selectively reset one itself in accordance with an instruction from the host processing means; and

a step of executing, by means of the reset central processing unit, the instruction code defined to be executed by the reset central processing unit itself, which is newly loaded in the internal storage means.

3. (Currently Amended) An information processing method realized in a system in which a processor including a plurality of central processing units, internal storage means, boot storage means, and a direct memory access controller, external storage means in which are stored a common code to be executed in common by the plurality of central processing units and an instruction code to be respectively executed by predetermined one of the central processing units, and host processing means are interconnected by a bus, the method characterized by comprising:

a step of selectively resetting, by means of the host processing means, the central processing unit;

a step of writing, by means of the host processing means, a boot code to be executed by the reset central processing unit into the boot storage means;

a step of canceling, by means of the host processing means, a reset state of the reset central processing unit;

a step of loading, by means of one of the central processing units of which the reset state is canceled, the common code and the instruction code defined to be executed by the one of the central processing units of which the reset state is canceled, into the internal storage means from the external storage means with the use of the direct memory access controller, by executing the boot code written in the boot storage means by the one of the central processing units of

which the reset state is canceled, and loading, by means of one of other central processing units of which the reset state is canceled, the instruction code defined to be executed by the one of other central processing units of which the reset state is canceled, into the internal storage means from the external storage means with the use of the direct memory access controller by executing the boot code written in the boot storage means by the one of other central processing units of which the reset state is canceled; and

a step of executing, by means of the respective central processing units of which the reset states are canceled, the common code and the instruction code defined to be executed by the respective central processing units of which reset states are canceled, which are loaded in the internal storage means,

wherein the common code, the instruction code loaded by the one of the central processing units, and the instruction code loaded by the one of the other central processing units share a common address space in the internal storage means.

4. (Original) The information processing method according to claim 3, further comprising:

a step of selectively newly resetting, by means of the host processing means, the central processing unit;

a step of writing, by means of the host processing means, a new boot code to be executed by the newly reset central processing unit into the boot storage means;

a step of canceling, by means of the host processing means, a reset state of the newly reset central processing unit;

a step of newly loading, by means of the central processing unit of which the reset state is canceled, the instruction code defined to be executed by the central processing unit of which the reset state is canceled into the internal storage means from the external storage means with the use of the direct memory access

controller by executing the new boot code by the central processing unit of which the reset state is canceled;

a step of executing, by means of the central processing unit of which the reset state is canceled, the instruction code defined to be executed by the central processing unit of which the reset state is canceled that is newly loaded in the internal storage means.

5. (Currently Amended) A program stored on a computer-readable medium for execution in a system in which a processor including a plurality of central processing units and internal storage means, external storage means in which are stored a common code to be executed in common by the plurality of central processing units and an instruction code to be respectively executed by predetermined one of the central processing units, and host processing means are interconnected by a bus, the program characterized by:

causing one of the central processing units to load the common code and the instruction code defined to be executed by one of the central processing units, into the internal storage means from the external storage means in accordance with an instruction from the host processing means, in accordance with an instruction from the host processing means and causing one of other central processing units to load the instruction code defined to be executed by the one of other central processing units, into the internal storage means from the external storage means; and

causing the respective central processing units to execute the common code and the instruction code defined to be executed by the respective central processing units, which are loaded in the internal storage means.

wherein the common code, the instruction code loaded by the one of the central processing units, and the instruction code loaded by the one of the other central processing units share a common address space in the internal storage means.

6. (Original) The program according to claim 5, further characterized by:

causing the host processing means to selectively reset the central processing unit;

causing the selectively reset central processing unit to newly load the instruction code defined to be executed by the reset central processing unit into the internal storage means from the external storage means in accordance with an instruction from the host processing means; and

causing the reset central processing unit to execute the newly loaded instruction code defined to be executed by the reset central processing unit.

7. (Currently Amended) A program stored on a computer-readable medium for execution in a system in which a processor including a plurality of central processing units, internal storage means, boot storage means, and a direct memory access controller, external storage means in which are stored a common code to be executed in common by the plurality of central processing units and an instruction code to be respectively executed by a predetermined one of the central processing units, and host processing means are interconnected by a bus, characterized by:

causing the host processing means to selectively reset the central processing unit;

causing the host processing means to write a boot code to be executed by the reset central processing unit into the boot storage means;

causing the host processing means to cancel a reset state of the reset central processing unit;

causing one of the central processing units of which the reset state is canceled to load the common code and the instruction code defined to be executed by one of the central processing units of which the reset state is canceled, into the internal storage means from the external storage means with the use of the direct memory access controller, by executing the boot code written in the boot storage means by one of the central processing units of which the reset state is canceled, and causing one of other central processing units of which the reset state is canceled to load the instruction code defined to be executed by the one of other central processing units of which the reset state is canceled, into the internal storage means from the external storage means with the use of the direct memory access controller by executing the boot code written in the boot storage means by the one of other central processing units of which the reset state is canceled; and

causing the respective central processing units of which the reset states are canceled to execute the common code and the instruction code defined to be executed by the respective central processing units of which the reset states are canceled, which are loaded in the internal storage means,

wherein the common code, the instruction code loaded by the one of the central processing units, and the instruction code loaded by the one of the other central processing units share a common address space in the internal storage means.

8. (Previously Presented) The program according to claim 7, further characterized by:

causing the host processing means to selectively newly reset the central processing unit;

causing the host processing means to write a new boot code to be executed by the newly reset central processing unit into the boot storage means;

causing the host processing means to cancel a reset state of the newly reset central processing unit;

causing the central processing unit of which the reset state is canceled to newly load the instruction code defined to be executed by the central processing unit of which the reset state is canceled into the internal storage means from the external storage means with the use of the direct memory access controller by executing the new boot code by the central processing unit of which the reset state is canceled;

causing the central processing unit of which the reset state is canceled to execute the instruction code defined to be executed by the central processing unit of which the reset state is canceled that is newly loaded in the internal storage means.

9. (Currently Amended) A recording medium in which a program is written, the program being executed in a system in which a processor including a plurality of central processing units and internal storage means, external storage means in which are stored a common code to be executed in common by the plurality of central processing units and an instruction code to be respectively executed by a predetermined one of the central processing units, and host processing means are interconnected by a bus, the recording medium characterized in that:

the program causes one of the central processing units to load the common code and the instruction code defined to be executed by one of the central processing units, into the internal storage means from the external storage means in accordance with an instruction from the host processing means, in accordance with an instruction from the host processing means and causing one of other central processing unit to load the instruction code defined to be executed by the one of other central processing units, into the internal storage means from the external storage means; and

the program causes the respective central processing units to execute the common code and the instruction code defined to be executed by the respective central processing units that are loaded in the internal storage means,

wherein the common code, the instruction code loaded by the one of the central processing units, and the instruction code loaded by the one of the other central processing units share a common address space in the internal storage means.

10. (Original) The recording medium according to claim 9, further characterized in that:

the program causes the host processing means selectively to reset the central processing unit;

the program causes the selectively reset central processing unit to newly load the instruction code defined to be executed by the reset central processing unit into the internal storage means from the external storage means in accordance with an instruction from the host processing means; and

the program causes the reset central processing unit to execute the newly loaded instruction code defined to be executed by the reset central processing unit.

11. (Currently Amended) A recording medium in which a program is written, the program being executed in a system in which a processor including a plurality of central processing units, internal storage means, boot storage means, and a direct memory access controller, external storage means in which are stored a common code to be executed in common by the plurality of central processing units and an instruction code to be respectively executed by predetermined one of the central processing units, and host processing means are interconnected by a bus, the recording medium characterized in that:

the program causes the host processing means to selectively reset the central processing unit;

the program causes the host processing means to write a boot code to be executed by the reset central processing unit into the boot storage means;

the program causes the host processing means to cancel a reset state of the reset central processing unit;

the program causes one of the central processing units of which the reset state is canceled to load the common code and the instruction code defined to be executed by one of the central processing units of which the reset state is canceled, into the internal storage means from the external storage means with the use of the direct memory access controller, by executing the boot code written in the boot storage means by one of the central processing units of which the reset state is canceled, and the program causes one of other central processing units of which the reset state is canceled to load the instruction code defined to be executed by the one of other central processing units of which the reset state is canceled, into the internal storage means from the external storage means with the use of the direct memory access controller by executing the boot code written in the boot storage means by the one of other central processing units of which the reset state is canceled; and

the program causes the respective central processing units of which the reset states are canceled to execute the common code and the instruction code defined to be executed by the respective central processing units of which the reset states are canceled, which are loaded in the internal storage means,

wherein the common code, the instruction code loaded by the one of the central processing units, and the instruction code loaded by the one of the other central processing units share a common address space in the internal storage means.

12. (Previously Presented) The recording medium according to claim 11, characterized in that:

the program causes the host processing means to newly selectively reset the central processing unit;

the program causes the host processing means to write a new boot code to be executed by the newly reset central processing unit into the boot storage means;

the program causes the host processing means to cancel a reset state of the newly reset central processing unit;

the program causes the central processing unit of which the reset state is canceled to newly load the instruction code defined to be executed by the central processing units of which the reset state is canceled, into the internal storage means from the external storage means with the use of the direct memory access controller, by executing the new boot code by the central processing units of which the reset state is canceled; and

the program causes the central processing unit of which the reset state is canceled to execute the instruction code defined to be executed by the central processing unit of which the reset states is canceled that is loaded in the internal storage means.